Annexure 1

Detailed Syllabus of Course

S. No	Module Title	Topics	Duration (Hours)		Learning Outcome
			Theory	Lab	
1.	**Introduction to Digital Electronics**	•Number System •Logic Gates •Latches and Flip Flops •Combinational Logic Circuit •Sequential Logic Circuit	4	6	• Basic athematic operation using binary numbers and the conversion. • Understanding of different types of gates and building logical circuit using basics and universal gates. • Knowledge of different types of flip-flop and latches and operation of combination and sequential circuit

2	**Basics of Digital VLSI Technology**	• **Basics of Digital VLSI Technology**
		  • Historical Perspective.
		  • VLSI technology trends performance measures and Moore's law comparisons of technology trends.
		  • Introduction to the family of Transistor.
		  • Basics of CMOS Transistor
		  • MOSFET Fabrication Process
		  • INVERTERS
		  • VLSI Design Flow
		  • Introduction to ASIC & FPGA
			4	8	• Understand brief history, present and future and Design Cycle of VLSI technology.
					• Understand the Design Cycle of VLSI

3	**Fabrication Process and Layout Design Rules**	• Fabrication Process and Layout Design Rules • Introduction to fabrication Process. • General Aspects of CMOS Technology. • CMOS Inverter Fabrication Process. • Layout Design Rules. • Semi-Custom Design Flow • Full-Custom Design Flow	6	0	• Understand Layout Design Rules. • Working principal, structure and operation of transistors like NMOS, PMOS and CMOS. • Understanding of fabrication Process MOSFET and CMOS devices.
4	**Digital CMOS Design**	• CMOS Inverter Basics. • Inverter Transfer Characteristics. • Inverter sizing. • Inverter Design. • Other types of Inverter and its problem.	4	8	• Understand the Digital CMOS Design • Design CMOS Inverter and analyze transfer characteristics • Types of inverter, their problem and solutions

5	**Hardware Modeling Using Verilog**	•Introduction to Verilog •Programming Structure •Level of Abstraction •Data Type •Behavioural Modelling and Timing •Verilog PROCEDURAL ASSIGNMENT •Introduction to BLOCKING NON-BLOCKING ASSIGNMENTS in Verilog •Verilog Functions •Verilog User Defined Primitives •Writing Very First Program •WRITING TEST BENCHES in Verilog •Verilog Simulation Basics	10	18	• Understand Verilog programming syntax. • Level of Abstraction in Verilog programing • Writing and simulating small programs and testbenches in Verilog
6	**Implementation and Simulation of Logic gates/circuits in Verilog using Tool (ModelSim or Xilinx)**	•Implementation of Logic Gates using Dataflow modelling in Verilog •Implementation of Universal Gates using Dataflow modelling in Verilog •Implementation of Logic Gates using Gate-Level Modelling in Verilog •Implementation of Universal Gates using Gate-Level modelling in Verilog •Implementation Mux in Verilog •Implementation different flip-flops in Verilog •Implementation Combinational Logic Circuit in Verilog •Implementation Sequential Logic Circuit in Verilog	2	20	•Implementation and Simulations of Basic, universal Gates using different modelling in Verilog •Implementation and Simulations of Mux (2:1, 4:1, 8:1) in Verilog. •Implementation and Simulations of Combinational and Sequential in Verilog
Total			**90 Hours(Theory-30, Practical-60)**		